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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete If Known

Application Number: 10/755,042

Filing Date: January 9, 2004

First Named Inventor: **MOU-SHIUNG LIN**

Art Unit: 2815

Examiner Name: **JEROME JACKSON, JR.**

Sheet

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of

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Attorney Docket No: 085027-0104

US PATENT DOCUMENTS

Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T*
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T*
	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
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	8	LEE, Y-H. et al. "Effect of ESD Layout on the Assembly Yield and Reliability," International Electron Devices Meeting (2006) pgs. 1-4	

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	9	YEOH, T-S. "ESD Effects On Power Supply Clamps," Proceedings of the 6th International Symposium on Physical & Failure Analysis of Integrated Circuits (1997) pgs. 121-124	
	10	EDELSTEIN, D. et al. "Full Copper Wiring in a Sub-0.25 µm CMOS ULSI Technology," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 773-776	
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	12	JENEI, S. et al. "High Q Inductor Add-on Module in Thick Cu/SiLK™ single damascene," Proceedings from the IEEE International Interconnect Technology Conference (2001) pgs. 107-109	
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	22	LUTHER, B. et al. "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices," Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference (1993) pgs. 15-21	
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	25	LIN, M.S. et al. "A New System-on-a-Chip (SOC) Technology - High Q Post Passivation Inductors," Proceedings from the 53rd Electronic Components and Technology Conference (05-30-2003) pgs. 1503-1509	
	26	MEGIC CORP. "MEGIC way to system solutions through bumping and redistribution," (Brochure) (02-06-2004) pgs. 1-3	
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